REMARKS

Status of the Claims

Claims 38-47 and 49 are pending, with Claims 38, 40, 42, 44, and 45 being independent. Claim 48 has been canceled.

Initially, Applicant would like to thank the Examiner for indicating that Claims 40-43 are allowed.

Applicant respectfully requests the Examiner to reconsider and withdraw the outstanding rejections in view of the following remarks.

Claim Objection

Claim 48 stands objected to under 37 C.F.R. § 1.75(c) as allegedly being of improper dependent form for failing to further limit the subject matter of a previous claim. Without conceding the propriety of the objection, Claim 48 has been deleted, thereby rendering this objection moot.

Claim Rejections Under 35 U.S.C. § 112

Claims 38, 39, 45-47, and 29 stand rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. This rejection is respectfully traversed.

The recited "$Ta_2(O_{1-x}N_x)_5$" refers to a tantalum oxide material containing nitrogen atoms. The present specification, at page 6, lines 24-26, discloses that "$Ta_2(O_{1-x}N_x)_5$ films can be prepared by thermal CVD or plasma-assisted CVD as described in U.S. Pat. No. 5,677,015."

U.S. Patent No. 5,677,015 (incorporated by reference in the present application at page 7, lines 7-8) discloses a tantalum oxynitride film made by chemical vapor deposition (Column 3, Lines 13-30) or by forming a tantalum-containing film and applying a plasma treatment using a gas containing nitrogen (Column 3, Lines 31-38) thereby providing 10 to 62.5 atomic % nitrogen atoms in the film (Column 4, Lines 22-25).

Applicant respectfully submits that the recited "$Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6" generally represents a tantalum oxide film having nitrogen incorporated therein.

In accordance with the indication given by the Examiner after a telephone conversation with the undersigned on February 16, 2004, during which the above points were discussed, withdrawal of the rejection is respectfully requested.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 38, 39, and 44-48 stand rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 5,880,508 ("Wu") in view of admitted prior art or U.S. Patent No. 4,947,081 ("Ohiwa"). This rejection is respectfully traversed.

Wu is cited as allegedly disclosing the steps of:

"forming an interfacial layer (6, fig. 1), comprising silicon nitride or silicon oxynitride, on a silicon semiconductor substrate; and

forming a high dielectric constant layer (8, fig. 1) on the interfacial layer[;]

forming a gate electrode of an electrically conductive material on the high dielectric constant layer; and

forming source and drain regions that are adjacent the gate electrode. (col. 2, lns. 63-67 and col. 3, lns. 1-22[])". (Official Action at page 2).

Wu relates to a method of fabricating a metal oxide semiconductor field effect transistor (MOSFET) with a permitivity gate dielectric. (Column 1, Lines 7-10). Wu discloses forming an ultra thin silicon oxynitride layer on the top surface of a single crystal silicon substrate. (Column 2, Lines 51-67). Wu further discloses depositing a thin dielectric layer with high permitivity by chemical vapor deposition on the silicon oxynitride layer. (Column 3, Lines 1-4). As disclosed by Wu, the dielectric layer can be chosen from a group of TiO_2, Ta_2O_5, PZT or BST, which have relatively high dielectric to silicon oxide, silicon nitride or the like. (Column 3, Lines 4-7).

Independent Claim 38 recites a method for fabricating a MOS device having a gate width of less than 0.3 micron comprising forming an interfacial layer on a semiconductor substrate. A high dielectric constant layer is formed on the interfacial layer, the high dielectric constant layer comprising $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, and wherein the interfacial layer separates the high dielectric constant layer from the substrate. A gate electrode of an electrically conductive material is formed on the high dielectric constant layer. Source and drain regions are formed in the substrate adjacent to the gate electrode.

Independent Claim 44 recites a method for fabricating a MOS device having a gate width of less than 0.3 micron comprising forming a silicon nitride interfacial layer on a semiconductor substrate. A high dielectric constant layer is formed on the silicon nitride interfacial layer, the high dielectric constant layer comprising a material that is selected from the group consisting of Ta_2O_5, a solid solution of $(Ta_2O_5)_r$-$(TiO_2)_{1-r}$ wherein r ranges from about 0.9 to less than 1, a solid solution $(Ta_2O_5)_s$-$(Al_2O_3)_{1-s}$ wherein s ranges from 0.9 to less than 1, and mixtures thereof wherein the silicon nitride interfacial layer separates the high dielectric constant layer from the substrate. A gate electrode of an electrically conductive material is formed on the high dielectric constant layer. Source and drain regions are formed in the substrate adjacent to the gate electrode.

Independent Claim 45 recites a method for fabricating a MOS device having a gate width of less than 0.3 micron comprising forming an interfacial layer on a semiconductor substrate. A high dielectric constant layer is formed on the interfacial layer, the high dielectric constant layer comprising a material selected from the group consisting of $Ta_2(O_{1-x}N_x)_5$ wherein x ranges from greater than 0 to 0.6, a solid solution of $(Ta_2O_5)_t$-$(ZrO_2)_{1-t}$ wherein t ranges from about 0.9 to less than 1, and a solid solution of $(Ta_2O_5)_u$-$(HfO_2)_{1-u}$ wherein u ranges from about 0.9 to less than 1, wherein the interfacial layer separates the high dielectric constant layer from the substrate. A gate electrode of an electrically conductive material is formed on the high dielectric constant layer. Source and drain regions are formed in the substrate adjacent to the gate electrode.

The Office Action acknowledges that Wu fails to disclose a high dielectric layer comprising $Ta_2(O_{1-x}N_x)_5$ and a gate width of less than 0.3 microns. Accordingly, the alleged admitted prior art on page 6, lines 24-26 of the present specification and Ohiwa are cited as allegedly disclosing that a high dielectric layer can be formed of $Ta_2(O_{1-x}N_x)_5$. (Office Action at page 2). Additionally, the Office Action alleges that "applicants' specification, page 7, line 25 – page 8, line 3, states that it is conventional for photoresist/lithography techniques to form a gate pattern that will form the line width of a gate less than 0.3 microns." (Office Action at page 3).

Applicant respectfully traverses the assertion in the Office Action that any prior art has been admitted. As noted above, the present specification, at page 6, lines 24-26, discloses that $Ta_2(O_{1-x}N_x)_5$ films, to be used in conjunction with the presently claimed methods for fabricating a MOS device, can be prepared by thermal CVD or plasma-assisted CVD as described in U.S. Pat. No. 5,677,015. Further, the disclosure at page 7, line 25 – page 8, line 3 of the present specification discloses embodiments of the presently claimed methods for fabricating a MOS device, ***not*** "conventional" photoresist/lithography techniques or "typical sizes when forming a gate electrode in the semiconductor art", as asserted in the Office Action. (see Office Action at page 3).

Ohiwa relates to a thin film electroluminescence device having dual insulation layers. (Column 1, Lines 8-9). A tantalum oxynitride layer is provided between a first insulation layer and a transparent electrode. (Column 1, Lines 57-68). Ohiwa discloses the

tantalum oxynitride as a transparent, high resistance semiconductor, as opposed to a high dielectric constant material. (Column 2, Lines 30-58).

"In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). MPEP § 2141.01(a).

Applicant respectfully submits that Ohiwa, related to a thin film electroluminescence device having dual insulation layers, is nonanalogous art that may not be relied upon as a basis for rejection of Applicant's invention.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP § 2143.

It is respectfully submitted that one skilled in the art would not be motivated to combine Wu, related to a method of fabricating a MOSFET with a permitivity gate dielectric, and Ohiwa, related to a thin film electroluminescence device having dual insulation layers.

As explained in MPEP § 2142, "The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness." It is respectfully submitted that if U.S. Patent No. 5,677,015 is to be relied upon for teachings pertaining to $Ta_2(O_{1-x}N_x)_5$, an explanation as to why one skilled in the art would be motivated to combine U.S. Patent No. 5,677,015 and Wu should be provided.

With regard to Claim 44, it is respectfully submitted that the combination of Wu and Ohiwa would not disclose or suggest all the claim limitations. Specifically, the combination of Wu and Ohiwa would not disclose or suggest a high dielectric constant layer on a silicon nitride interfacial layer. Further, the combination of Wu and Ohiwa would not disclose or suggest a gate width of less than 0.3 microns.

Accordingly, for at least the above-noted reasons, it is respectfully submitted that the Office Action has not set forth a *prima facie* case of obviousness. Accordingly, withdrawal of the rejection is respectfully requested.

Conclusion

For the reasons noted above, the art of record does not disclose or suggest the inventive concept of the presently claimed invention as defined by the claims.

In view of the foregoing remarks, reconsideration of the claims and allowance of the subject application is earnestly solicited. The Examiner is invited to contact the undersigned at the below-listed telephone number, if it is believed that prosecution of this application may be assisted thereby.

Respectfully submitted,

BURNS, DOANE, SWECKER & MATHIS, L.L.P.

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By: _____
Asaf Batelman
Registration No. 52,600

P.O. Box 1404
Alexandria, Virginia 22313-1404
(703) 836-6620